UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/762,981	05/09/2001	Andrea Olgiati	B-4089PCT	1339

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EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/30/2007 and 10/27/2005*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 14-18* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All · b)☐ Some * c)☒ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   In view of the Appeal Brief filed on July 30, 2007, PROSECUTION IS HEREBY

REOPENED. A new rejection has been formulated as set forth below.

2.   To avoid abandonment of the application, appellant must exercise one of the

following two options:

        (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply

under 37 CFR 1.113 (if this Office action is final); or,

        (2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed

by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and

appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth

in 37 CFR 41.20 have been increased since they were previously paid, then appellant

must pay the difference between the increased fees and the amount previously paid.

3.   A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by

signing below:
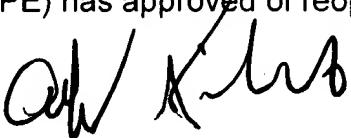
                                    **ALFORD KINDRED
                                    SUPERVISORY PATENT EXAMINER**

Priority

4.   Acknowledgment is made of applicant's claim for foreign priority based on an

application filed in the European Patent Office on June 15, 1999. It is noted, however,

that applicant has not filed a certified copy of the European application as required by

35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the
> United States before the invention thereof by the applicant for patent, or on an international application
> by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this
> title before the invention thereof by the applicant for patent.

6.   The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act

of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior

to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7.   Claims 1-3, 5-9 and 14-18 are rejected under 35 U.S.C. 102(e) as being

anticipated by Webb et al., US Patent by 6,061,749 (herein after referred to as Webb).

8.   Referring to claim 1, Webb has taught a computer system, comprising:

    a.   a first processor (Figure 4, element 202);

    b.   a second processor for use as a coprocessor to the first processor (Figure

4, element 224);

    c.   a coprocessor controller (column 12, lines 15-62, Figure 5, at least

elements 1030, 1031 and 1032, and Figure 4, element 4, elements 202 and 1022

all comprise a coprocessor controller that controls the coprocessor.);

    d.   a memory (Figure 4, element 203); and

    e.   a decoupling element (Figure 4, element 1022, column 13, lines 4-7);

f.   wherein computations are passed to the second processor from the first

processor through the decoupling element, such that the second processor

executes computations passed from the first processor through the decoupling

element (column 12, lines 27-35), and wherein the second processor receives

data from and writes data to the memory (column 12, lines 15-26), and wherein

the coprocessor controller controls the activity of the second processor to ensure

execution of the second processor is correctly ordered with respect to loads from

memory (column 12, lines 15-62, Figure 5, at least elements 1030, 1031 and

1032, and Figure 4, element 4, elements 202 and 1022 all comprise a

coprocessor controller that controls the coprocessor to ensure that the

coprocessor is correctly ordered with respect to loads and stores to /from

memory.), whereby the execution of computations by the second processor is

decoupled from the operation of the first processor such that the second

processor executes computations passed from the first processor through the

decoupling element while the first processor is providing further instructions to

the decoupling element (Figure 4, element 1022 is the decoupling element where

the instructions from the CPU 202 are passed and queued up while instructions

execute in the coprocessor 224.).

9.   Referring to claim 2, Webb has taught a computer system as claimed in claim 1,

as described above, and wherein the decoupling element is a coprocessor instruction

queue, wherein computations are added to the coprocessor instruction queue by the

first processor and consumed from the coprocessor instruction queue by the

coprocessor (Figure 4, element 1022, column 12, lines 27-35).

10.   Referring to claim 3, Webb has taught a computer system as claimed in claim 1,

as described above, and wherein the decoupling element is a state machine, wherein

information to provide computations to the second processor is provided to the state

machine by the first processor, and computations are provided in an ordered sequence

to the second processor by the state machine (Figure 4, element 1022, column 12, lines

27-35, Element 1022 is a state machine.).

11.   Referring to claim 5, Webb has taught a computer system as claimed in claim

1, as described above, and wherein the second processor is configurable (column

18, line 66-column 19, line 16, configuration and status registers in the

coprocessor).

12.   Referring to claim 6, Webb has taught a computer system as claimed in claim

5, as described above, and wherein the second processor is adapted to be

configured in accordance with a configuration downloaded from the memory

(column 18, line 66-column 19, line 16, Configuration information is downloaded

into the configuration and status registers.).

13.   Referring to claim 7, Webb has taught a computer system as claimed in claim 1,

as described above and wherein the first processor is able to switch tasks during

execution of computations by the second processor (Figure 4, Since processors 202

and 224 are separated by a queue 1022, then when CPU 202 passes instructions to

1022 for buffering, then the co-processor executes the instructions while the CPU 202 is able to switch to another task.).

14.   Referring to claim 8, Webb has taught a computer system as claimed in claim 1, as described above, and further comprising

    a.   a buffer memory from which the second processor loads data and to which the second processor stores data, wherein the buffer memory is adapted to load data from the memory and store data to the memory (Figure 6, elements 1040 and 1041 comprise the claimed buffer memory for storing and loading instructions from memory.).

15.   Referring to claim 9, Webb has taught a computer system as claimed in claim 8, as described above, and wherein the memory is dynamic random access memory, and the buffer memory is adapted to load data from, or store data to, the buffer memory in bursts (column 14, lines column 14, lines 40-67, a predetermined number of instructions are added to the queue.).

16.   Referring to claim 14, Webb has taught a computer system as claimed in claim 8, as described above, and further comprising

    a.   a synchronisation mechanism to synchronise transfer of data between the buffer memory and the memory with execution of computations by the second processor (column 14, lines 28-39).

17.   Referring to claim 15, Webb has taught the computer system as claimed in claim 14, as described above, and wherein the synchronisation mechanism is

adapted to block execution of computations by the second processor on data

which has not yet been loaded to the buffer memory from the memory, and is

adapted to block execution of memory instructions for storage of data from the

buffer memory to the memory where relevant computations have not yet been

executed by the second processor (column 12, lines 316-62).

18.   Referring to claim 16, Webb has taught a computer system as claimed in

claim 15, as described above, and adapted such that when execution of

computations or memory instructions is blocked by the synchronisation

mechanism, other computations or memory instructions which are not blocked by

the synchronization mechanism may be executed (column 12, lines 16-62,

Subsequent instructions that depend on executing instructions are blocked.

Instructions that are not depended on any prior instructions may be executed.).

19.   Referring to claim 17, Webb has taught a computer system as claimed in claim 1,

as described above, and wherein the first processor is the central processing unit of a

computer device (Figure 4, element 202 is a CPU).

20.   Referring to claim 18, Webb has taught a method of operating a computer

system, comprising:

        a.   providing code for execution by a first processor and a second processor

        acting as coprocessor to the first processor (Figure 4, where element 202 is the

        first processor and element 224 is the coprocessor);

b.   identifying a part of the code as providing a task to be carried out by the

second processor (column 12, lines 27-35);

c.   passing information defining the task from the first processor to a

decoupling element (column 12, lines 27-35, instructions are passed to the

queue 1022, column 13, lines 4-7); and

d.   passing instructions derived from said information from the decoupling

element to the second processor and executing said instructions on the second

processor (column 12, lines 27-35), wherein the processing of said instructions

by the second processor is decoupled from the operation of the first processor

such that the second processor executes said instructions passed from the

decoupling element while the first processor passes further information defining

the task to the decoupling element (Figure 4, element 1022 is the decoupling

element where the instructions from the CPU 202 are passed and queued up

while instructions execute in the coprocessor 224.).

Claim Rejections - 35 USC § 103

21.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

22.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et

al., US Patent 6,061,749 (herein after Webb) in view of Kim, US Patent 6,052,713

(herein after Kim).

23.   Referring to claim 4, Webb has taught a computer system as claimed in claim 1,

as described above. Webb has not specifically taught that the decoupling element is a

third processor, wherein information to provide computations to the second processor is

provided to the third processor by the first processor, and computations are provided in

an ordered sequence to the second processor by the third processor. However, Kim

has taught such a concept for the desirable purpose of implementing a cellular system

(Figure 1, column 4, lines 7-27). Therefore it would have been obvious to one of

ordinary skill in the art at the time the invention was made to have the decoupling

element of Webb be a third processor, such that information to provide computations to

the second processor is provided to the third processor by the first processor, and

computations are provided in an ordered sequence to the second processor by the third

processor for the desirable purpose of implementing a cellular system.

Allowable Subject Matter

24.   Claims 10-13 are objected to as being dependent upon a rejected base claim,

but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims.

Conclusion

25.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

26.   A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

27.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tonia L. Meonske whose telephone number is (571)

272-4170. The examiner can normally be reached on Monday-Friday with first Friday's

off.

28.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

29.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLM

/Tonia L. Meonske/
Tonia L. Meonske
October 18, 2007